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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/538,684
Filing Date: March 30, 2000
Appellant(s): KINSMAN ET AL.

James R. Duzan
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9-13-7 appealing from the Office action mailed 3-21-7.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,994,936	HERNANDEZ	2-1991
5,696,031	WARK	12-1997
5,136,471	INASAKA	8-1992
JP5102338	NAKAMURA	4-1993

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

Claims 1-4, 6, 8, 11, 12, 14-16, 18-20, 24-29, 31, 33, 36, 37 and 39-45 stand rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hernandez (4994936).

In the abstract and column 1, lines 6-12; 22-56; column 2, lines 4-17, and 21-64; column 3, line 62 to column 4, line 23; column 4, line 49 to column 6, line 2; column 6, line 35 to column 7, line 61; column 8, lines 59-

63; column 9, lines 16-18; and column 10, lines 7-10, Hernandez discloses the following:

An integrated circuit package having a plurality of leads 16 and a heat sink 60, 68, the plurality of leads having reduced lead inductance "minimize inductance in the leads" from that of a conventional electrically isolated heat sink, "The decoupling scheme of the present invention provides many features and advantages relative to prior art decoupling schemes. For example, the close proximity between the decoupling capacitor and IC chip provides noise decoupling with very low inductance" comprising: a package body 27; an integrated circuit die 28 positioned within the package body; a lead frame 10 including a plurality of leads 16 having portions enclosed within the package body that connect to the integrated circuit die (via 30, 32), the plurality of leads having portions enclosed within the package body forming an area; and an electrically conductive heat sink 60/60', 68 positioned at least partially within the package body with a surface of a first portion (portion of 60 from top of 66 to distance equal to thickness of 70) and 70 of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body "The surface area of capacitor 34 may be equal to, less than, or greater than the surface area of die platform 22. Preferably,

however, capacitor 34 will have a larger surface area (as shown in FIGS. 5 and 6) which extends beyond the die support platform. This larger surface area of the capacitor 34 will act to both minimize inductance in the leads from the lead frame as well as to increase the capacitor's heat sink capabilities. It will be appreciated that the size of the capacitor is only limited by the distance between the dam bars 18 of the lead frame (see FIG. 1)" and with a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink, the heat sink directly coupled to one of a signal voltage and a reference voltage the heat sink operating respectively as a signal plane and a ground plane for the plurality of leads of the lead frame, "conductor 38 will have leads which will be attached to the corresponding voltage or ground leads of the lead frame" reducing lead inductance of the plurality of leads of the lead frame inherently at least about 0.90 nanoheneries [sic]; wherein the package body includes one of a transfer molded plastic package body and a preformed ceramic package body; wherein the integrated circuit die includes one of a Dynamic Random Access Memory integrated circuit die, a Static Random Access Memory integrated circuit die, a Synchronous Dynamic Random Access Memory integrated circuit die, a Sequential Graphics Random Access Memory

integrated circuit die, a flash Electrically Erasable Programmable Read-Only Memory integrated circuit die, and an inherent processor integrated circuit die; wherein the lead frame includes one of a peripheral-lead finger lead frame, a Leads Over Chip lead frame, and a Leads Under Chip lead frame; wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection; wherein the heat sink is positioned only partially within the package body "said stem terminates at a surface which is exterior of said molding material"; wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame; wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body; wherein the first and second portions of the heat sink are integral with one another; wherein the first and second portions of the heat sink comprise separate parts; wherein the heat sink comprises a plurality of parts 60, 70, each forming a portion of both the first and second portions of the heat sink; wherein the heat sink has locking holes 64, 74, 78, 84 therein for locking the heat sink in the integrated circuit package; further comprising an adhesive attaching the lead frame to the heat sink; wherein the integrated circuit package comprises one

of a Vertical Surface Mount Package, a Small Outline J-lead package, a Thin Small Outline Package, a Quad Flat Pack, and a Thin Quad Flat Package.

An integrated circuit package having a plurality of leads and a heat sink, the plurality of leads having a reduced lead inductance comprising: a package body; an integrated circuit die positioned within the package body; a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area; an electrically conductive heat sink positioned at least partially within the package body with a vertically extending columnar portion 60' surrounded by a horizontally extending skirt portion 34 having a vertical thickness, said columnar portion having a vertical thickness which is greater than the vertical thickness of said skirt portion, and having a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion, the lead frame attachment surface being attached to the lead frame and extending in close proximity to a substantial part of the enclosed portions of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body, the die-attach surface being attached to the integrated circuit die reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries.

An integrated circuit package having heat sink and a plurality of leads having a reduced lead inductance comprising: an integrated circuit die; a lead frame including a plurality of leads having portions that are connected to the integrated circuit die, the plurality of leads forming an area; and an electrically conductive heat sink positioned having a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of an enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink, the heat sink coupled to one of a signal voltage and a reference voltage for the heat sink to operate respectively as a signal plane and a ground plane for the plurality of leads of the lead frame reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries; a package body; wherein the package body includes one of a transfer molded plastic package body and a preformed ceramic package body; wherein the integrated circuit die includes one of a Dynamic Random Access Memory integrated circuit die, a Static Random Access Memory integrated circuit die, a Synchronous Dynamic Random Access Memory integrated circuit die, a Sequential Graphics Random Access Memory integrated circuit die, a flash

Electrically Erasable Programmable Read-Only Memory integrated circuit die, and a processor integrated circuit die; wherein the lead frame includes one of a peripheral-lead finger lead frame, a Leads Over Chip lead frame, and a Leads Under Chip lead frame; wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a "welded" connection; wherein the heat sink is positioned only partially within the package body; wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame; wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body; wherein the first and second portions of the heat sink are integral with one another; wherein the first and second portions of the heat sink comprise separate parts; wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink;, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located; wherein the heat sink has locking holes therein for locking the heat sink in the integrated circuit package; further comprising an adhesive attaching the lead frame to the heat sink; wherein the integrated circuit package comprises one of a Vertical Surface Mount

Package, a Small Outline J-lead package, a Thin Small Outline Package, a Quad Flat Pack, and a Thin Quad Flat Pack.

To further clarify the disclosure of the process of using the heat sink directly coupled to one of a signal voltage and a reference voltage the heat sink operating respectively as a signal plane and a ground plane for the plurality of leads of the lead frame reducing lead inductance of the plurality of leads of the lead frame inherently at least about 0.90 nanoheneries, in the instant specification, paragraphs 32 and 33, appellant discloses that the particular claimed inductance is an inherent result of the process of using the claimed package: "The first portion 26 of the heat sink 28 extends beneath a substantial part of enclosed portions 32 of the leads 16 of the lead frame 18 in close proximity to the leads 16 but separated therefrom by an adhesive insulative layer 38, such as an adhesive tape or screen printed adhesive on the lead frame 18 or the heat sink 28. By extending in such close proximity to the leads 16, the first portion 26 of the heat sink 28 magnetically couples to the leads 16 and reduces the mutual and self inductance associated with the leads 16 as described above. A first portion 26 that extends beneath a 'substantial part' of the enclosed portions 32 of the leads 16 includes, but is not limited to, those first portions that extend beneath substantially all of the enclosed portions of the leads 16, that extend substantially to sides 33 of the IC package 10 as shown in FIG. 1A,

and that, for example, extend beneath at least about eighty percent (80%) of the area of the enclosed portions of the lead frame 18." "Such results have also shown that in another IC package in which the heat sink of the present invention is connected to a signal voltage, lead inductance is reduced from that of a conventional heat sink connected to a signal voltage by about 25 percent (from about 4.60 nH to about 3.47 nH)." Furthermore, as elucidated supra, Hernandez discloses a process of using the package with the heat sink directly coupled to one of a signal voltage and a reference voltage the heat sink operating respectively as a signal plane and a ground plane for the plurality of leads of the lead frame reducing lead inductance of the plurality of leads of the lead frame. Therefore, in the process of using the package of Hernandez, inductance of the plurality of leads of the lead frame is inherently at least about 0.90 nanoheneries.

To further clarify, Hernandez discloses an inherent processor integrated circuit die because Hernandez discloses the following processor integrated circuit die functions: "It is well known in the field of microelectronics that high frequency operation, particularly the switching of integrated circuits, can result in transient energy being coupled into the power supply circuit. It is also well known that integrated circuits are becoming more dense (more gates per unit area of silicon/or gallium arsenide), more powerful (more watts per unit area of IC chip), and faster

with higher clock rate frequencies and with smaller rise times. All of these recent and continued developments make the problem of suppressing noise in the power bus (produced by a large amount of simultaneous gates switching) even more serious than in the past."

In the alternative, claims 1-4, 6, 8-12, 14-20, 22, 24-29, 31-37 and 39-45 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez (4994936).

Hernandez is applied as it is applied to claims 1-4, 6, 8-12, 14-20, 22, 24-29, 31-37 and 39-45 supra.

However, Hernandez does not appear to explicitly disclose the process of using the package by reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries.

Notwithstanding, Hernandez discloses that lead inductance is a result-effective variable. Therefore, it would have been obvious to try variations of the inductance result effective variable, including the claimed variations because "a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense." KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007). See also, Pfizer Inc. v. Apotex Inc., 82 USPQ2d 1852 (Fed. Cir. 2007). Moreover, as reasoned from well established legal

precedent, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed lead inductance in the process of using the package because appellant has not disclosed that, in view of the applied prior art, the particular inductance is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another process. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can

rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims .... In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results."

Further in the alternative, claims 1-4, 6, 8, 11, 12, 14-16, 18-20, 24-29, 31, 33, 36, 37 and 39-45 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez as applied to claims 1-4, 6, 8, 11, 12, 14-16, 18-20, 24-29, 31, 33, 36, 37 and 39-45 supra, and further in combination with Wark (5696031).

Hernandez does not appear to disclose literally a "processor."

Still, at column 2, lines 47-63; column 3, lines 9-11; and column 5, lines 59-65, Wark discloses a "processor." In addition, it would have been obvious to combine this disclosure of Wark with the disclosure of Hernandez because it would facilitate provision of the device of Hernandez.

Claims 9 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez as applied to claim 1, and further in combination with Inasaka (5136471).

As cited, Hernandez discloses wherein a heat sink is coupled to a printed circuit board outside the package body thereby coupled to one of a signal voltage and a reference voltage; wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

However, Hernandez does not appear to explicitly disclose wherein the heat sink is coupled to a printed circuit board outside the package body thereby coupled to one of a signal voltage and a reference voltage.

Nevertheless, as cited, Hernandez discloses wherein a heat sink 34 is coupled by leads 16 to a "circuit board" outside the package body thereby coupled to one of a signal voltage and a reference voltage. Further, at column 2, lines 53-68; and column 4, lines 17-30, Inasaka discloses wherein a package body 30 is coupled to a "printed circuit board" outside the package body thereby coupled to one of a "signal voltage" and a "reference voltage." Moreover, it would have been obvious to combine these disclosures of the applied prior art because it would facilitate provision of the circuit board, signal voltage and reference voltage of the embodiment of Hernandez applied to claim 1.

In the alternative, claims 9 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez and Inasaka as applied to claims 9 and 10 supra, and further in combination with Wark (5696031).

Wark is applied for the same reasons it is applied supra.

Claim 17 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez as applied to claim 1, and further in combination with Nakamura (JP5102338).

Hernandez does not appear to explicitly disclose wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located. Regardless, in the English abstracts and Figure 3, Nakamura discloses wherein the surface of the first portion of the heat sink 1 includes a recess 7 in which the die-attach area is located. Furthermore, it would have been obvious to combine this disclosure of Nakamura with the disclosure of Hernandez because it would facilitate the heat transmission of Hernandez, enable die alignment and adhesive containment, and as disclosed by Inasaka, it would hold the die, reduce mounting height, increase mounting density, enable plating bar cutting and reduce cost.

In the alternative, claim 17 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez and Nakamura as applied to claim 17 supra, and further in combination with Wark (5696031).

Wark is applied for the same reasons it is applied supra.

Claim 22 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez as applied to claim 1, and further in combination with Wark (5696031).

As cited, Hernandez discloses an integrated circuit package having a plurality of leads and a heat sink, the plurality of leads having reduced lead inductance comprising a package body; an integrated circuit die positioned within the package body; a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area; and an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body forming an area and having a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink and the integrated circuit die for reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries.

However, Hernandez does not appear to explicitly disclose an electronic system having an input device, an output device, a memory device, and a processor device coupled to the input, output, and memory devices, at least one of the input, output, memory, and processor devices. Nevertheless, as cited supra, Wark teaches these limitations. Moreover, it would have been obvious to combine this disclosure of Wark with the disclosure of Hernandez because it provide low inductance devices in the system of Wark, and facilitate provision of the device of Hernandez.

Claims 34 and 35 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez as applied to claim 26, and further in combination with Inasaka (5136471).

As cited, Hernandez discloses wherein the heat sink is coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame; wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

However, Hernandez does not appear to explicitly disclose wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby coupled to one of a signal voltage and a reference voltage.

Nevertheless, as cited, Hernandez discloses wherein a heat sink 34 is coupled by leads 16 to a "circuit board" outside the package body thereby

coupled to one of a signal voltage and a reference voltage. Further, at column 2, lines 53-68; and column 4, lines 17-30, Inasaka discloses wherein a package body 30 is coupled to a "printed circuit board" outside the package body thereby coupled to one of a "signal voltage" and a "reference voltage." Moreover, it would have been obvious to combine these disclosures of the applied prior art because it would facilitate provision of the circuit board, signal voltage and reference voltage of the embodiment of Hernandez applied to claim 26.

In the alternative, claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hernandez and Inasaka as applied to claim 34 and 35 supra, and further in combination with Wark (5696031).

Wark is applied for the same reasons it is applied supra. Appellant's remarks filed 11-28-6 have been fully considered and are moot in view are the new grounds of rejection.

(10) Response to Argument

Appellant asserts, "the decoupling capacitor 34, 68 of Hernandez cannot be the 'electrically conductive heat sink' element of the claimed invention as recited in claim 1."

This assertion is respectfully traversed because Hernandez explicitly discloses, "Still another important feature of this invention is an improvement in heat transfer from the IC chip out of the molded package.

Presently, heat is conducted out of the package primarily through the molding compound from the silicon chip. By attaching the decoupling capacitor to the lead frame, an improvement in heat conduction results in that the capacitor acts as a heat spreader by dispersing heat from the IC chip to the molding compound through a larger cross-section. This feature becomes more prominent when the area of the decoupling capacitor conductors is larger than that of the IC die support platform. Also, because of the space taken up by the capacitor, any heat will have less plastic package to pass through in order to exit the package. In a preferred embodiment, additional improvement in heat transfer is achieved by use of a heat sink plug."

Also, appellant alleges, "the decoupling capacitor 34, 68 of Hernandez does not have a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die as recited in claim 1. Instead, the decoupling capacitor 34, 68 of Hernandez is attached to the heat sink and lead frame, but not the IC chip 28. (Hernandez, col. 7, lines 31-33)."

This allegation is respectfully traversed because appellant merely cites without elucidation and the citation does not otherwise appear to support the allegation. Moreover, Hernandez clearly discloses the claimed die-attach area, e.g. attached to 66 in Figures 16 and 21. In any case, the scope of

the claims is not limited to the die-attach area directly attached to the integrated circuit die and Hernandez discloses the die-attach area at least indirectly attached to the die.

Appellant also states, "The Examiner acknowledges that Hernandez fails to disclose 'reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries.' (March 21, 2007, Office Action, page 16).

This statement is respectfully traversed because there is no acknowledgement that Hernandez fails to disclose reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries as cited or elsewhere in the record. Instead, is maintained that "Hernandez does not appear to explicitly disclose reducing lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries."

In addition, appellant contends, "The Examiner cites no authority for the proposition that such a decoupling capacitor would reduce 'lead inductance of the plurality of leads of the lead frame at least about 0.90 nanoheneries.'"

This contention is respectfully traversed because ample authority is cited for the disclosure of this limitation. To this end, MPEP 2112 V recites:

> ONCE A REFERENCE TEACHING PRODUCT APPEARING TO BE SUBSTANTIALLY IDENTICAL IS MADE THE BASIS OF A REJECTION, AND THE EXAMINER PRESENTS EVIDENCE OR REASONING TENDING TO SHOW INHERENCY, THE BURDEN SHIFTS TO THE APPLICANT TO SHOW AN UNOBVIOUS DIFFERENCE

> "[T]he PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his [or her] claimed product. Whether the rejection is based on inherency' under 35 U.S.C. 102, on prima facie obviousness' under 35 U.S.C. 103, jointly or alternatively, the burden of proof is the same...[footnote omitted]." The burden of proof is similar to that required with respect to product-by-process claims. In re Fitzgerald, 619 F.2d 67, 70, 205 USPQ 594, 596 (CCPA 1980) (quoting In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977)).

MPEP 2113 recites:

> ONCE A PRODUCT APPEARING TO BE SUBSTANTIALLY IDENTICAL IS FOUND AND A 35 U.S.C. 102 /103 REJECTION MADE, THE BURDEN SHIFTS TO THE APPLICANT TO SHOW AN UNOBVIOUS DIFFERENCE
>
> "The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. In re Fessmann, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974).
>
> Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. In re Marosi, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983).

Therefore, appellants contention is respectfully deemed unpersuasive because there is no requirement for a citation of extrinsic evidence. Moreover, a rationale, namely, the ability to be used in the claimed process of using the package, is provided tending to show that the claimed product appears to be the same or similar to that of the prior art.

The remaining arguments are adequately treated in the Examiner's answer supra.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

David E. Graybill

Conferees:

Darren E. Schuberg

Michael Lebentritt